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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/774,178 | YEUNG ET AL. | |
| | Examiner | Art Unit | |
| | CAROLINE ARCOS | 2195 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,7,10-15,19,39-41 and 44-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,10-15,19,39-41 and 44-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/06/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/18/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-4, 7, 10-15, 19, 39-41, 44-50 are pending for examination.

### *Continued Examination Under 37 CFR 1.114*

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/18/2009 has been entered.

### *Claim Objections*

3. Claim 7 is objected to because it is dependent on a cancelled claim 6. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-4, 7, 10-15, 19, 39-41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the

application was filed, had possession of the claimed invention.

5. The following limitations ("determining the availability of configurable hardware components" and "dynamically adjusting the buffer size based at least on the state of the application and the state of the threads") contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Examiner interprets the second limitation as dynamically adjusting the configurable hardware components in the system based at least on the state of the application and the state of the threads.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-4, 7, 10-15, 19, 39-41, 44-50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The claim language in the following claims is not clearly understood:

i. As per claim 1, lines 8-9, it is unclear how the coordination of the thread dispatch increase execution overlap of the threads, It is unclear what is the criteria in the dispatch process that increase the execution overlap of the threads.

ii. As per claim 14, it has the same deficiency as claim 1.

iii. As per claim 39, it has the same deficiency as claim 1.

iv. As per claim 44, it is unclear what is the relation between the plurality of threads and the application (i.e. are the plurality of threads part of the application).

v. As per claim 48, it has the same deficiency as claim 44.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 7, 11-14, 19, 39, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Yavatkar et al. (US 2003/0137945 A1) and further in view of Armstrong et al. (US 2004/0216113 A1).

8. As per claim 1, Zaccarin teaches the invention substantially as claimed including a method, comprising:

monitoring a state of an application running in a system, including monitoring one or more buffers associated with the application ([0013]; par. [0014], lines 15-23; par. [0015], lines 4-12; par. [0017]; par. [0019]; par. [0021]);

monitoring a machine state of the system, including determining the availability of configurable hardware components in the system, wherein the configurable hardware

components include at least a processor and a buffer ([0013]; par. [0014]; par. [0015]; par. [0019]; par. [0020]);

wherein at least one of the threads is associated with the application (par. [0013; par. [0014]; par. [0015])

9. Zaccarin does not explicitly teach that the processor that performs simultaneous multi-threading ; coordinating dispatch of a plurality of threads in the system at least in part to increase execution overlap of the threads, and dynamically adjusting the buffer size based at least on the state of the application and the state of the threads in the system, dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads.

10. However, Yavatkar dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads and dynamically adjusting the buffer size based at least on the state of the application and the state of the threads in the system (fig. 4; par. [0018]; par. [0020]; [0021]).

11. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Yavatkar because Yavatkar teaching of dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads and taking into consideration the buffer level would be well known to one of ordinary skill in

the art of due to monitoring buffer levels, managing the energy of the processor taking into the account the state of the threads that can be manipulated in adjusting the buffer levels.

12. The combined teaching Zaccarin and Yavatkar does not explicitly the processor that performs simultaneous multi-threading; coordinating dispatch of a plurality of threads in the system at least in part to increase execution overlap of the threads.

13. However, Armstrong teaches the processor that performs simultaneous multi-threading; coordinating dispatch of a plurality of threads in the system at least in part to increase execution overlap of the threads (par. [0004]; par. [0006]; par. [0011]).

14. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar and Armstrong because Armstrong teaching of simultaneous multi-threading which increase overlapping of multiple threads execution at one time.

15. As per claim 7, Zaccarin teaches the configurable hardware components further include hardware buffers, memory, cache, arithmetic logic unit (ALU), and registers in the system (par. [0019], lines 4-9; par. [0021]; lines 9-13).

16. As per claim 11, Zaccarin teaches said monitoring the one or more buffers associated with the application includes monitoring buffer fullness levels of the one or

more buffers (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16; par. [0016], lines 10-12; par. [0018]).

17. As per claim 12, Zaccarin teaches said monitoring the buffer fullness levels includes, for each buffer associated with the application, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0015], lines 8-16; Par. [0017]; par. [0018]).

18. As per claim 13, Zaccarin teaches said comparing is to determine buffer overflow and buffer underflow conditions (par. [0015], lines 4-16; par. [0017], lines 4-15).

19. As per claim 14, it is the computer readable storage medium of the method claim 1. Therefore, it is rejected under the same rational.

20. As per claim 19, Zaccarin teaches said monitoring the buffer fullness levels includes, for each buffer associated with the application, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16; par. [0016], lines 10-12; par. [0017]; par. [0018]).

21. As per claim 39, Zaccarin teaches a system, comprising:

a memory to store data and instructions (fig. 4,42; par. [0042);

a processor ; said processor operable to perform instructions (fig. 4, 56);

monitor a state of an application running in a system, including monitoring buffer fullness levels of one or more buffers associated with the application (par. [0013]; par. [0014]);

monitoring a machine state of the system, including determining the availability of configurable hardware components in the system, wherein the configurable hardware components include at least a processor and a buffer ([0013]; par. [0014]; par. [0015]; par. [0019]; par. [0020]);

wherein at least one thread is associated with the application (par. [0013]; par. [0014]; par. [0015]);

22. Zaccarin does not explicitly teach a processor coupled to said memory on a bus, said processor comprising:

a bus unit to receive a sequence of instructions from said memory;

an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions, a processor that performs simultaneous multi-threading; coordinate dispatch of a plurality of threads in the system at least in part to increase execution overlap of the threads, dynamically adjust one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads; and dynamically adjusting the buffer size based at least on the state of the

application and the state of the threads in the system.

23. However, Yavatkar dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads and dynamically adjusting the buffer size based at least on the state of the application and the state of the threads in the system (fig. 4; par. [0018]; par. [0020]; [0021]).

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Yavatkar because Yavatkar teaching of dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads and taking into consideration the buffer level would be well known to one of ordinary skill in the art of due to monitoring buffer levels, managing the energy of the processor taking into the account the state of the threads that can be manipulated in adjusting the buffer levels.

25. The combined teaching Zaccarin and Yavatkar does not explicitly the processor that performs simultaneous multi-threading; coordinating dispatch of a plurality of threads in the system at least in part to increase execution overlap of the threads.

26. However, Armstrong teaches the processor that performs simultaneous multi-threading; coordinating dispatch of a plurality of threads in the system at least in part to

increase execution overlap of the threads (par. [0004]; par. [0006]; par. [0011]).

27. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar and Armstrong because Armstrong teaching of simultaneous multi-threading which increase overlapping of multiple threads execution at one time.

28. The combined teaching of Zaccarin, Yavatkar and Armstrong does not explicitly teach a processor coupled to said memory on a bus, said processor comprising:

a bus unit to receive a sequence of instructions from said memory;

an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions.

29. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching that a processor coupled to said memory on a bus, said processor comprising: a bus unit to receive a sequence of instructions from said memory; an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions since it is well known to one of ordinary skill in the art that the processor is coupled to some sort of memory to receive the instruction to be executed.

30. As per claim 41, Zaccarin teaches that said execution unit to monitor a machine state of the system, wherein said monitoring the machine state includes: increasing or

decreasing the configurable hardware components available in the system based on the state of the application and the state of the one or more threads in the system (par. [0014]; par. [0015]; par. [0017]).

31. Zaccarin does not explicitly teach determining resources available in the system. However, Armstrong teaches determining resources available in the system (abs; par. [0012]).

32. Claims 2-4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Yavatkar et al. (US 2003/0137945 A1), in view of Armstrong et al. (US 2004/0216113 A1) as applied to claim 1 and 14 above, and further in view of Kling et al. (US 6,662,203 B1).

33. As per claim 2, the combined teaching of Zaccarin, Yavatkar and Armstrong does not explicitly teach a thread includes one or more activities, and wherein said coordinating dispatch of the threads in the system includes assessing execution readiness of the one or more activities.

34. However, Kling teaches a thread includes one or more activities, and wherein said controlling the dispatch of the threads in the system includes assessing execution readiness of the one or more activities (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

35. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar, Armstrong and kling because Kling teaching of accessing readiness of the one or more activities improve system dispatching techniques and increase efficiency in dispatching technique of the system since one would only be dispatching ready activities only which improve the performance of the system.

36. As per claim 3, Kling teaches said controlling the dispatch of the one or more threads in the system includes delaying a ready-to-be-dispatched activity from being dispatched (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

37. As per claim 4, Zaccarin teaches the first and second activities are from one or more applications (par. [0012]; par. [0021]).

38. The combined teaching of Zaccarin, Yavatkar and Armstrong does not explicitly teach that a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

39. However, Kling teaches a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

40. As per claim 15, it is the computer readable medium of the method claim 3. Therefore it is rejected under the same rational.

41. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Yavatkar et al. (US 2003/0137945 A1), in view of Armstrong et al. (US 2004/0216113 A1) as applied to claim 1 above, and further in view of Jain et al. (US 2002/0188884 A 1).

42. As per claim 10, the combined teaching of Zaccarin, Yavatkar and Armstrong does not explicitly teach that said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system.

43. However, Jain teaches said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system (par. [0040]; claim 1).

44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar, Armstrong and Jain because Jain teaching of said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system would improve system energy consumption and increase efficiency.

45. Claim 40, 44-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Yavatkar et al. (US 2003/0137945 A1) and further in view of Armstrong et al. (US 2004/0216113 A1), and further in view of Kling et al. (US 6,662,203 B1).

46. As per claim 40, the combined teaching of Zaccarin, Yavatkar and Armstrong does not explicitly teach that said controlling the dispatch of the one or more threads in the system includes delaying a ready- to-be-dispatched thread from being dispatched.

47. However, Kling teaches said controlling the dispatch of the one or more threads in the system includes delaying a ready-to-be-dispatched thread from being dispatched(abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1- 15; fig. 5).

48. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar, Armstrong and kling since Kling teaching of delaying a ready-to-be- dispatched thread from being dispatched would improve system throughput and increase efficiency of system resource usage.

49. As per claim 44, Zaccarin teaches a system, comprising:

processor (fig. 4, 56);

a resource manager coupled to processor (fig. 4);

the resource manager is to monitor states of an application running in the system, the states of the application including buffer fullness levels of one or more buffers used by the application,(par. [0013]; par. [0014]; par. [0015]; par. [0017]; par. [0021]).

50. Zaccarin does not explicitly teach a multi-threading processor; and the resource manager is to further monitor states of a plurality of threads in the system for execution readiness and the resource manager is to increase or decrease resources available in the system depending on the state of the application and/or the states of the one or more threads in the system.

51. However, Yavatkar teaches the resource manager is to increase or decrease resources available in the system depending on the state of the application and/or the states of the one or more threads in the system (fig. 4; par. [0018]; par. [0020]; [0021]).

52. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Yavatkar because Yavatkar teaching of dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads and taking into consideration the buffer level would be well known to one of ordinary skill in the art of due to monitoring buffer levels, managing the energy of the processor taking into the account the state of the threads that can be manipulated in adjusting the buffer levels.

53. The combined teaching Zaccarin and Yavatkar does not explicitly teach a multi-threading processor and the resource manager is to further monitor states of a plurality of threads in the system for execution readiness.

54. However, Armstrong teaches a multi-threading processor (par. [0004]; par. [0006]; par. [0011]).

55. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar and Armstrong because Armstrong teaching of simultaneous multi-threading which increase overlapping of multiple threads execution at one time.

56. The combined teaching of Zaccarin, Yavatkar and Armstrong does not explicitly teach the resource manager is to further monitor states of a plurality of threads in the system for execution readiness.

57. However, kling teaches the resource manager is to further monitor states of a plurality of threads in the system for execution readiness (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

58. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar and Armstrong and Kling because

Kling teaching of monitor states of one or more threads in the system for execution readiness would improve dispatching and scheduling techniques and system performance by monitoring ready thread to dispatch them.

59. As per claim 45, Kling teaches that wherein the resource manager is to change the execution readiness of a thread from a ready state to a queued state to increase subsequent thread execution overlap with execution of another thread (col. 2, lines 10-16).

60. As per claim 46, Kling teaches change the execution readiness of a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1- 24; col. 9, lines 38-col. 10, lines 1-15).

61. The combined teaching of Zaccarin, Yavatkar and Armstrong and Kling does not explicitly teach that the change is to increase subsequent system idle time when there is no thread execution. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Kling teaching of batch system and changing from ready to queued state that beside increasing the efficiency in using the system resource, it is increasing subsequent system idle time when there is no thread execution which improve the system throughput by processing the threads in a parallel at once.

62. As per claim 47, Zaccarin teaches the resource manager is to increase or decrease the resources available in the system to avoid buffer underflow or overflow conditions to occur to the one or more buffers (par. [0013]; par. [0014]; par. [0015]par.[0017]).

63. As per claim 48. Zaccarin teaches an apparatus, comprising:

logic to monitor states of an application running in a system, the states of the application including buffer fullness levels of one or more buffers used by the application (abs., lines 9-12; col. 2, lines 29-32; col. 2, lines 62-66; col. 12, lines 18-28; par. [0015], lines 4-16; par. [0017], lines 4-15); and a memory to store the logic (par. [0024]).

64. Zaccarin does not explicitly teach a processor capable of simultaneous multi-threading, logic to adjust resources available in the system depending on the state of the application and/or the states of the threads in the system and logic to monitor states of a plurality of threads in the system for execution readiness.

65. However, Yavatkar teaches logic to adjust resources available in the system depending on the state of the application and/or the states of the threads in the system fig. 4; par. [0018]; par. [0020]; [0021]).

66. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Yavatkar because Yavatkar teaching of dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads and

taking into consideration the buffer level would be well known to one of ordinary skill in the art of due to monitoring buffer levels, managing the energy of the processor taking into the account the state of the threads that can be manipulated in adjusting the buffer levels.

67. The combined teaching Zaccarin and Yavatkar does not explicitly teach a processor capable of simultaneous multi-threading, and logic to monitor states of a plurality of threads in the system for execution readiness.

68. However, Kling teaches logic to monitor states of one or more threads in the system for execution readiness (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

69. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar and Kling because Kling teaching of monitoring the execution readiness of one or more thread would improve Zaccarin system performance and dispatching techniques by knowing that one or more threads are ready to be executed, one would be able to take the steps necessary to dispatch them.

70. The combined teaching of Zaccarin, Yavatkar and Kling does not explicitly teach a processor capable of simultaneous multi-threading. However, Armstrong teaches a processor capable of simultaneous multi-threading (par. [0004]; par. [0006]; par. [0011]).

71. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar, Kling and Armstrong because Armstrong teaching of simultaneous multi-threading which increase overlapping of multiple threads execution at one time.

72. As per claim 49, Kling teach logic to change the execution readiness of a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

73. The combined teaching of Zaccarin, Yavatkar, Kling and Armstrong does not explicitly teach that the change in state is when it is determined that there is no other thread running or ready to be dispatched.

74. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching and especially Kling teaching that the ready threads are moved to wait queue until the batch is complete to be dispatched so it would have been obvious that the first thread in the ready queue is moved to the wait queue until other ready threads becomes ready and join the first thread in the wait queue, when they will be dispatched.

75. As per claim 50, Zaccarin teaches that the logic to adjust the available resources in the system includes logic to determine if the buffer fullness levels of one or more

buffers are in a critical stage (par.[0015]; par. [0017]).

***Response to Arguments***

76. Applicant's arguments with respect to claims 1-4, 7, 10-15, 19, 39-41, 44-50 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

77. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

78. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

79. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

80. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Caroline Arcos/
Examiner, Art Unit 2195

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195